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selected from the group consisting of silicon dioxide, silicon nitride, silicon oxynitride, hafnium oxide, and zirconium oxide.

10. (original) The method of claim 1 wherein said opening in said dielectric region is lined with dielectric spacers, said dielectric spacers having been formed on sidewalls of said sacrificial gate.

11. (original) The method of claim 10 wherein said dielectric spacers include L-shaped oxide spacers having sidewalls exposed at said opening and overlying nitride spacers.

12. (currently amended) A method of fabricating a field effect transistor (FET), comprising:

forming a source region and a drain region in a semiconductor substrate and a sacrificial gate disposed between a pair of spacers ~~over a~~ overlying said semiconductor ~~region of a~~ substrate, said ;

~~forming a~~ source region and said ~~a~~ drain region being disposed on opposite sides of said sacrificial gate;

forming a dielectric layer on said substrate having a top surface generally planar to a top of said sacrificial gate;

removing said sacrificial gate to form an opening between said pair of spacers, said opening extending to said semiconductor region;

forming a gate dielectric on said semiconductor region in said opening;

forming a first conductive layer in said opening including at least one material

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selected from the group consisting of metals and compounds of metals;

B depositing a layer of silicon on said first conductive layer in said opening;

removing said dielectric layer and forming a second metal layer including a silicide-forming metal over said source region and said drain region and said layer of silicon; and

annealing said substrate to form a silicide from said silicide-forming metal, said silicide contacting said source region and said drain region and contacting said layer of silicon.

13. (currently amended) The method of claim 12 wherein said annealing also forms a silicide at an interface between said first ~~metal~~ conductive layer and said layer of silicon.

14. (original) The method of claim 13 wherein said silicide-forming metal includes at least one metal selected from the group consisting of cobalt, nickel, titanium and platinum.

15-20. (cancelled)

21. (new) The method of claim 13, wherein said first layer is separated from said semiconductor substrate only by a thickness of said gate dielectric.